HERITAGE INSTITUTE OF TECHNOLOGY

TIME TABLE

<Electronics & Communication Engineering >

M. Tech 2nd Year 2nd Semester (VLSI) **SESSION: 2022-2023**

DAY	GROUP	9.00 AM – 9.55 AM	9.55 AM – 10.50 AM	10.50 AM – 11.45 AM	11.45 AM – 12.25 PM	12.25 PM – 1.20 PM	1.20 PM – 2.15 PM	2.15 PM – 3.10 PM	3.10 PM – 4.05 PM	4.05 PM – 5.00 PM	5.00 PM – 5.55 PM
MON	GR. 1	Project/ VLSI 6295/ ICT 602				Project/ VLSI 6295/ ICT 602					
	GR. 2										
TUE	GR. 1	Project/ VLSI 6295/ ICT 602									
	GR. 2										
WED	GR. 1	Project/ VLSI 6295/ ICT 604				Project/ VLSI 6295/ ICT 602					
	GR. 2										
THU	GR. 1	Project/ VLSI 6295/ ICT 604									
	GR. 2										
FRI	GR. 1	Project/ VLSI 6295/ ICT 602				Project/ VLSI 6295/ ICT 602					
	GR. 2										

To be Effective from 9th January, 2023.

A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination

Students should target 100% attendance

Asima Adak

Member

HOD

Principal

HERITAGE INSTITUTE OF TECHNOLOGY

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<Electronics & Communication Engineering >

M. Tech 2nd Year 2nd Semester (VLSI) **SESSION: 2022-2023**

COURSE STRUCTURE:

2nd. Year, Semester II

Sl. No.	Course Type	Code	Course Title	Contact Hours/Week				Credits
				L	T	P	Total	
1	Dissertation	VLSI6295	Dissertation Phase-II	0	0	32	32	14
2	Grand Viva	VLSI6297	Comprehensive Viva Voce	-	-	-	-	2
Total of Semester				**0**	**0**	**32**	**32**	**16**

To be Effective from 9th January, 2023.

A minimum of 75% attendance is mandatory for being eligible to sit for the End-Semester Examination

Students should target 100% attendance

Asima Adak

Member

HOD

Principal